Day : Wednesday

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Date: 8/31/2005
Time: 10:11:14

Inventor Name Search Result

Your Search was:

Last Name = DABRAL
First Name = SANJAY

Application#	Patent#	Status	Date Filed	Title	Inventor Name
08662618	5781258	150	06/13/1996	ASSEMBLING AND SEALING LARGE, HERMETIC AND SEMI-HERMETIC, H-TILED, FLAT-PANELED DISPLAYS	DABRAL, SANJAY
08938359	6154498	150	09/26/1997	COMPUTER SYSTEM WITH A SEMI-DIFFERENTIAL BUS SIGNALING SCHEME	DABRAL, SANJAY
08940303	6090650	150	09/30/1997	METHOD TO REDUCE TIMING SKEWS IN I/O CIRCUITS AND CLOCK DRIVERS CAUSED BY FABRICATION PROCESS TOLERANCES	DABRAL, SANJAY
08962812	5953521	150	11/03/1997	DATA-PATTERN INDUCED SKEW REDUCER	DABRAL, SANJAY
08994083	5973526	150	12/19/1997	COMPENSATING A CHARACTERISTIC OF A CIRCUIT	DABRAL, SANJAY
08997223	6043682	150	12/23/1997	PREDRIVER LOGIC CIRCUIT	DABRAL, SANJAY
09001550	6192431	150	12/31/1997	A METHOD APPARATUS FOR CONFIGURING THE PINOUT OF AN INTEGRATED CIRCUIT	DABRAL, SANJAY
09007658	6249329	250	01/15/1998	ASSEMBLING AND SEALING LARGE, HERMETIC AND SEMI-HERMETIC H-TILE FLAT PANEL DISPLAY	DABRAL, SANJAY
09052883	6175253	150	03/31/1998	FAST BI-DIRECTIONAL TRISTATEABLE LINE DRIVER	DABRAL, SANJAY
09094886	6370498	150	06/15/1998	APPARATUS AND METHOD FOR MULTI-LINGUAL USER ACCESS	DABRAL, SANJAY

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Inventor Name Search Result

Your Search was:

Last Name = CANAGASABY
First Name = KARTHISHA

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10334276	6788155	150	12/31/2002	LOW GAIN PHASE-LOCKED LOOP CIRCUIT	CANAGASABY, KARTHISHA
10890332	Not Issued	71	07/13/2004	Low gain phase-locked loop circuit	CANAGASABY, KARTHISHA
11094810	Not Issued	30	03/31/2005	Pre-drivers for current-mode I/O drivers	CANAGASABY, KARTHISHA
09951750	Not Issued	41	09/13/2001	Method and apparatus to emulate IO interconnection	CANAGASABY, KARTHISHA S.
09982242	Not Issued	30	10/16/2001	Method and apparatus to emulate external IO interconnection	CANAGASABY, KARTHISHA S.
10284245	Not Issued	30	10/31/2002	Receiver tracking mechanism for an I/O circuit	CANAGASABY, KARTHISHA S.
10404622	Not Issued	41	03/31/2003	On-die pattern generator for high speed serial interconnect built-in self test	CANAGASABY, KARTHISHA S.
10610316	Not Issued	30	06/30/2003	I/O link with configurable forwarded and derived clocks	CANAGASABY, KARTHISHA S.
11171114	Not Issued	20	06/30/2005	Serial link apparatus, method, and system	CANAGASABY, KARTHISHA S.

Inventor Search Completed: No Records to Display.

Search Another: Inventor Last Name: canagasaby First Name: karthisha Search

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09107351	6137143	150	06/30/1998	DIODE AND TRANSISTOR DESIGN FOR HIGH SPEED I/O	DABRAL, SANJAY
09256843	6278312	150	02/24/1999	METHOD AND APPARATUS FOR GENERATING A REFERENCE VOLTAGE SIGNAL DERIVED FROM COMPLEMENTARY SIGNALS	DABRAL, SANJAY
09336486	6243272	150	06/18/1999	METHOD AND APPARATUS FOR INTERCONNECTING MULTIPLE DEVICES ON A CIRCUIT BOARD	DABRAL, SANJAY
09368639	6356115	150	08/04/1999	CHARGE SHARING AND CHARGE RECYCLING FOR AN ON-CHIP BUS	DABRAL, SANJAY
09451684	6777975	150	11/30/1999	INPUT-OUTPUT BUS INTERFACE TO BRIDGE DIFFERENT PROCESS TECHNOLOGIES	DABRAL, SANJAY
09467300	6373715	150	12/17/1999	ORIENTING MULTIPLE PROCESSORS ON TWO SIDES OF A PRINTED CIRCUIT BOARD	DABRAL, SANJAY
09470686	6453422	150	12/23/1999	REFERENCE VOLTAGE DISTRIBUTION FOR MULTILOAD I/O SYSTEMS	DABRAL, SANJAY
09473855	6480059	150	12/28/1999	A METHOD TO REDUCE TIMING SKEWS IN I/O CIRCUITS AND CLOCK DRIVERS CAUSED BY FABRICATION PROCESS TOLERANCES	DABRAL, SANJAY
09474345	Not Issued	161	12/29/1999	INLINE AND "Y" INPUT-OUTPUT BUS TOPOLOGY	DABRAL, SANJAY
09474564	6704277	150	12/29/1999	TESTING FOR DIGITAL SIGNALING	DABRAL, SANJAY
09475648	6515534	150	12/30/1999	ENHANCED CONDUCTIVITY BODY BIASED PMOS DRIVER	DABRAL, SANJAY
09476585	6417688	150	12/31/1999	METHOD AND APPARATUS FOR IMPLEMENTING A HIGHLY ROBUST, FAST, AND ECONOMICAL FIVE LOAD BUS TOPOLOGY BASED ON BIT MIRRORING AND A WELL TERMINATED TRANSMISSION ENVIRONMENT	DABRAL, SANJAY
09539666	6622256	150	03/30/2000	SYSTEM FOR PROTECTING	DABRAL, SANJAY

				STROBE GLITCHES BY SEPARATING A STROBE SIGNAL INTO POINTER PATH AND TIMING PATH, FILTERING GLITCHES FROM SIGNALS ON POINTER PATH THEREOF	
09596613	6417462	150	06/19/2000	LOW COST AND HIGH SPEED 3 LOAD PRINTED WIRING BOARD BUS TOPOLOGY	DABRAL, SANJAY
09608449	6601196	150	06/29/2000	METHOD AND APPARATUS FOR DEBUGGING TERNARY AND HIGH SPEED BUSSES	DABRAL, SANJAY
09609434	6646324	150	06/30/2000	METHOD AND APPARATUS FOR A LINEARIZED OUTPUT DRIVER AND TERMINATOR	DABRAL, SANJAY
09651385	Not Issued	83	08/29/2000	Diode and transistor design for high speed I/O	DABRAL, SANJAY
09748233	6715111	150	12/27/2000	METHOD AND APPARATUS FOR DETECTING STROBE ERRORS	DABRAL, SANJAY
09848996	6434016	150	05/04/2001	AN APPARATUS FOR INTERCONNECTING MULTIPLE DEVICES ON A CIRCUIT BOARD	DABRAL, SANJAY
09935421	6670558	150	08/22/2001	INLINE AND "Y" INPUT-OUTPUT BUS TOPOLOGY	DABRAL, SANJAY
09935470	Not Issued	161	08/22/2001	Inline and "Y" input-output bus topology	DABRAL, SANJAY
09935512	6624717	150	08/22/2001	IMPEDANCED MATCHED BUS TRACES OVER DE-GASSING HOLES	DABRAL, SANJAY
09951750	Not Issued	41	09/13/2001	Method and apparatus to emulate IO interconnection	DABRAL, SANJAY
09962716	6507219	150	09/21/2001	CHARGE SHARING AND CHARGE RECYCLING FOR AN ON-CHIP BUS	DABRAL, SANJAY
09963439	6561820	150	09/27/2001	SOCKET PLANE	DABRAL, SANJAY
09982242	Not Issued	30	10/16/2001	Method and apparatus to emulate external IO interconnection	DABRAL, SANJAY
09993575	6905526	150	11/06/2001	FABRICATION OF AN ION EXCHANGE POLISH PAD	DABRAL, SANJAY
09993807	6722950	150	11/06/2001	METHOD AND APPARATUS FOR ELECTRODIALYTIC	DABRAL, SANJAY

				CHEMICAL MECHANICAL POLISHING AND DEPOSITION	
09993809	6773337	150	11/06/2001	METHOD AND APPARATUS TO RECONDITION AN ION EXCHANGE POLISH PAD	DABRAL, SANJAY
10116503	6561410	150	04/03/2002	LOW COST AND HIGH SPEED 3 LOAD PRINTED WIRING BOARD BUS TOPOLOGY	DABRAL, SANJAY
10136011	6594769	150	04/29/2002	REFERENCE VOLTAGE DISTRIBUTION FOR MULTILOAD I/O SYSTEMS	DABRAL, SANJAY
10232157	Not Issued	41	08/30/2002	Increasing robustness of source synchronous links by avoiding write pointers based on strobes	DABRAL, SANJAY
10262359	Not Issued	30	09/30/2002	Method and system for improved phase tracking	DABRAL, SANJAY
10284245	Not Issued	30	10/31/2002	Receiver tracking mechanism for an I/O circuit	DABRAL, SANJAY
10314308	6639450	150	12/09/2002	ENHANCED CONDUCTIVITY BODY BIASED PMOS DRIVER	DABRAL, SANJAY
10314309	6661277	150	12/09/2002	ENHANCED CONDUCTIVITY BODY BIASED PMOS DRIVER	DABRAL, SANJAY
10330598	6922071	150	12/27/2002	SETTING MULTIPLE CHIP PARAMETERS USING ONE IC TERMINAL	DABRAL, SANJAY
10334276	6788155	150	12/31/2002	LOW GAIN PHASE-LOCKED LOOP CIRCUIT	DABRAL, SANJAY
10334935	Not Issued	30	12/31/2002	Phase/frequency detector for tracking receivers	DABRAL, SANJAY
10394977	Not Issued	41	03/20/2003	Method and apparatus for a linearized output driver and terminator	DABRAL, SANJAY

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